18 May 2026

dorsaVi Resolves Key Materials Barrier, Marking Major Milestone to 22nm RRAM Commercialisation

The result removes the materials risk and positions dorsaVi to manufacture its RRAM on standard commercial foundry lines at scale.

Key Highlights:

- **Three material stacks qualified:** All three RRAM material stacks have passed commercial foundry Back-End-of-Line (BEOL) compatibility testing. Qualifying three distinct candidates rather than one reduces single-stack risk and gives the engineering team flexibility in selecting the final production stack.
- **Compatible with standard CMOS production:** All three stacks integrate with existing commercial foundry processes, meaning the technology can be manufactured on standard CMOS production lines without requiring a bespoke process or dedicated facility.
- **De-risked 180nm to 22nm pathway:** The 180nm test chip is a deliberate validation step rather than a workaround with Tape-out at a Tier-1 commercial foundry targeted for Q3 2026 and 22nm design phase commencing in H2 2027. The phased approach mitigates integration risk before scaling to the commercial node.
- **Pre-tape-out work complete:** Both the RRAM and the Compute-in-Memory (CIM) circuit and layout designs are complete. Formal design review is scheduled for June 2026, with Layout-versus-Schematic verification confirmed on the MAC array and test keys.
- **22nm scaling opens commercial markets:** The 22nm node delivers higher cell density, lower energy per operation, and improved thermal robustness compared with 180nm. These gains bring exoskeletons, prosthetics, medical implants, and industrial robotics into commercial scope.
- **Compute-in-Memory integrated:** The Company's manufacturing partner has completed the circuit design and layout for a CIM macro running directly on the 256Kb RRAM array. Executing inference inside the memory array removes the energy cost of shuttling data to a separate processor and reduces decision latency**.**
- **Direct enabler of dorsaVi's wearable robotics strategy:** This RRAM platform is the hardware foundation behind the Company's smart sensor strategy. It is what allows dorsaVi's FDA-cleared sensors to evolve from raw-data streaming devices into autonomous, on-body inference nodes.

- **Commercial manufacturing economics:** The BEOL-stacked architecture uses standard CMOS lines rather than a dedicated facility, which is what supports cost-effective, high-volume production economics.

Melbourne, Australia, 18 May 2026 – dorsaVi Limited (ASX: DVL) ("dorsaVi" or "the Company") is pleased to announce a major materials engineering breakthrough, validating the commercialisation pathway for its 22nm RRAM scale-down program. The company has successfully validated three advanced RRAM materials with standard commercial foundry processes, establishing a highly de-risked and credible foundation for the Company's migration to the high value 22nm node.

This milestone addresses the primary bottleneck in edge computing, the energy-intensive separation of memory and processing units. By validating a compute-in-memory (CIM) architecture, dorsaVi is shifting the industry standard toward a low-power, autonomous model that allows sensors to process complex data locally and act in real-time. This breakthrough accelerates the Company's "Ultra Edge Intelligence" strategy, transforming its FDA-cleared movement sensors into intelligent, on-body inference nodes for the multi-billion-dollar global robotics and medical device markets.

The Commercial Gateway: Validating the Three Pillars of RRAM Success

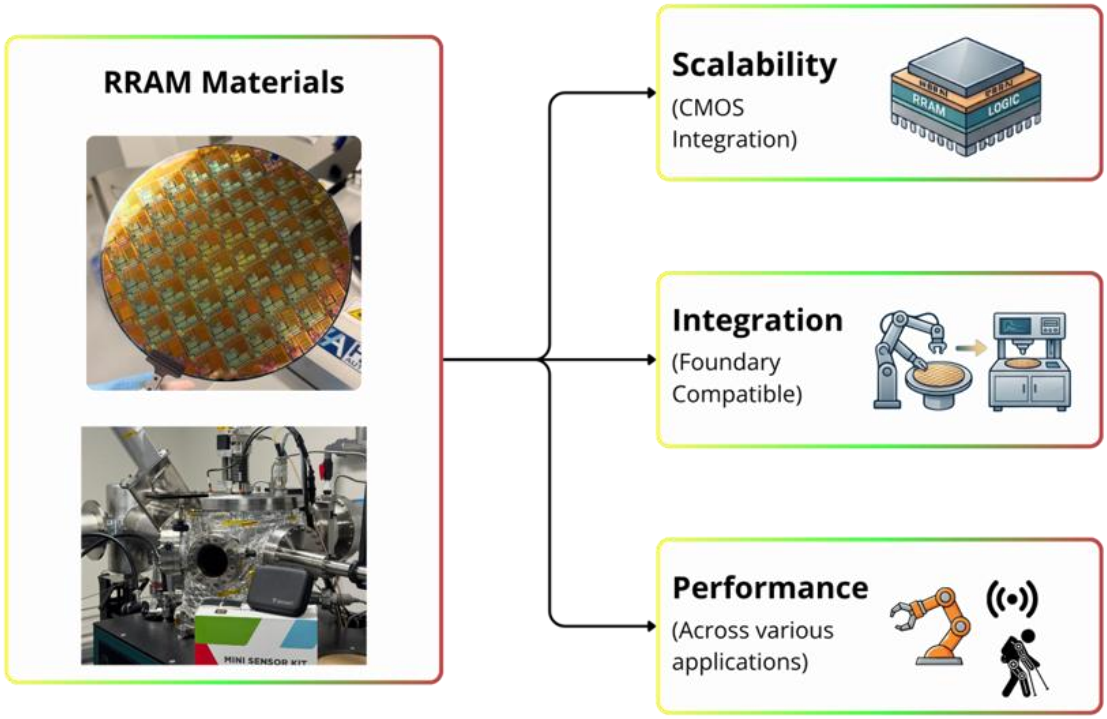

Figure 1: RRAM Material Qualification Framework establishing the Foundation for Commercial Scalability, CMOS Integration, and a De-risked Path to 22nm Production.

RRAM (Resistive Random Access Memory) is a high-endurance, low-power, non-volatile memory that enables in-memory computing for edge devices. However, its commercial success depends entirely on Back-End-of-Line (BEOL) compatibility, the ability to integrate into standard silicon foundries without requiring bespoke equipment or modified processes. In semiconductor manufacturing, a "stack" is the

vertical arrangement of thin-film material layers, typically a switching medium sandwiched between electrodes, that forms each individual memory cell.

Three parameters determine whether an RRAM stack is commercially viable:

- **Scalability (Foundry Fit):** The stack must use standard deposition, and etching tools already present in high-volume foundries. If a technology requires unique machinery, the capital expenditure becomes a barrier to entry.

- **Integration (CMOS Compatibility):** Materials must be CMOS-compatible, surviving the foundry's thermal budgets and chemical etching processes without degradation. Seamless integration onto standard CMOS wafers ensures high yields and lower costs by avoiding dedicated production lines.

- **Performance (Application Target):** Material composition dictates the device's operational envelope. By optimizing write voltage, endurance, and uniformity, the technology can be tailored for specific high-growth sectors from ultra-low-power wearables to robust automotive controllers and high-density AI compute arrays.

The team has now **cleared all three parameters** across three different stacks. By successfully qualifying three distinct material stacks against these rigorous criteria, the team has effectively de-risked the manufacturing roadmap. This achievement bridges the gap between RRAM's theoretical promise and high-volume commercial production, clearing a direct path for migration to the high value 22nm node.

With these benchmarks cleared, the Company is now positioned to tailor its RRAM technology for high-growth sectors, delivering the speed, density and thermal robustness required for high-value applications such as, **exoskeletons**, **industrial robotics**, and advanced **AI compute arrays**.

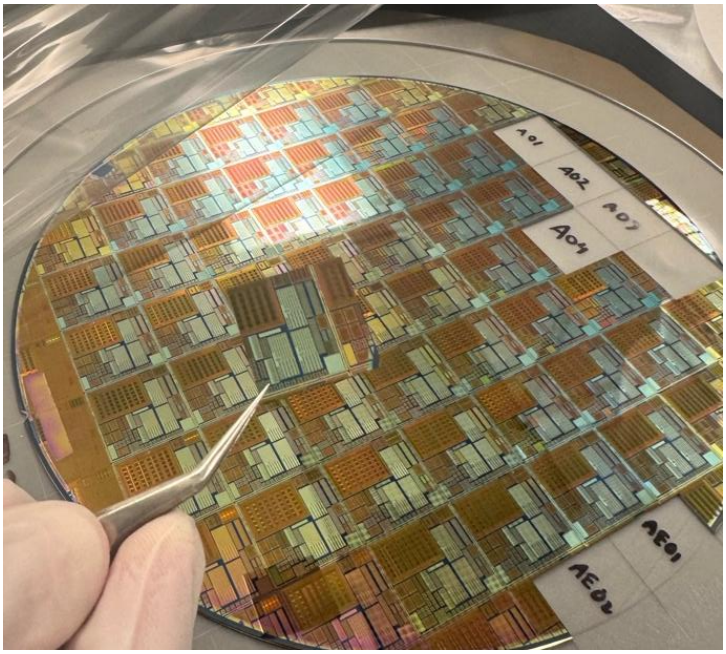

Figure 2: the Companies RRAM being verified and tested in the lab

Strategic Collaboration and Manufacturing Ecosystem

The 22nm RRAM program is being executed through a highly integrated, multi-year collaboration with world-leading research and manufacturing partners. This consortium, previously detailed in the Company's **ASX announcement dated 28 January 2026**, combines proprietary device-level innovation with Tier-1 foundry services and advanced circuit co-design expertise.

The Company has strategically opted for a phased development roadmap, first validating the technology on a mature 180nm process before scaling directly to the high value 22nm node.

This approach is designed to:

- **Ensure Scalability**: Aligning materials with standard foundry tools early in the process.
- **Mitigate Risk:** Closing the technical gap between material science and functional silicon integration.
- **Maximize Yield**: Establishing a stable foundation for cost-effective, high-volume production.

The 22nm CMOS node serves as the immediate follow-on step once the current test vehicle returns from the foundry. Operational alignment between all parties remains on a strict bi-weekly cadence, ensuring rapid technical iteration and a clear path toward commercialisation.

Material Engineering Progress

dorsaVi and its partners have qualified three RRAM material stacks. All three have passed the Back-End-of-Line (BEOL) compatibility tests required to integrate RRAM directly on top of standard CMOS wafers.

This is the commercial milestone the company's program has been working toward, demonstrating that the RRAM layers can survive the thermal budgets and chemical processes of a standard foundry without degrading the silicon underneath, which is the technical condition for commercial-grade manufacturing.

The recent testing phase has yielded specific technical data confirming the readiness of these qualified stacks for high-volume production:

Development Milestone	Technical Achievement	Commercial Impact
Low-Power Operation	Stable sub-1V DC switching demonstrated across all three qualified stacks	Meets the low-voltage requirement for battery-powered and energy-harvesting edge devices
Process Qualification	Three testing phases closed: etch study, particle scan, and BEOL compatibility short-loop	Confirms process cleanliness and manufacturing stability using standard foundry tools

Simulation Readiness	Cell variation characterised and integrated into the circuit simulation environment	Gives engineering teams the data they need to model real-world performance and yield
Path to Integration	BEOL thermal budget met; stacks ready for 1T1R (one transistor, one resistor) integration and AC testing	Moves the project out of materials testing and into functional memory array development

Why BEOL Compatibility Matters for 22nm

The fundamental differentiator of the Company's RRAM platform is its **Back-End-of-Line (BEOL)** integration. While traditional memory architectures often require a complex and costly redesign of the foundational silicon layers, DVL's RRAM is added directly to the final metal layers of standard CMOS wafers.

This "layered" approach makes the technology intrinsically **node portable**. Because the manufacturing conditions remain remarkably consistent across different chip generations, the compatibility work successfully completed at this stage translates directly to more advanced node sizes.

The successful testing of these material stacks has confirmed:

- **Structural Integration:** Material candidates were successfully layered and integrated using standard, high-volume manufacturing techniques.
- **Process Resilience:** All qualified stacks maintained full stability and performance when exposed to standard commercial foundry thermal and chemical environments.
- **Production Maturity:** Verified compatibility with standard industrial cleaning and smoothing processes, ensuring the architecture is ready for high-yield commercial production.

By validating this BEOL-compatible architecture, the Company has established a highly de-risked foundation for its migration to the high-value 22nm market. This transition is expected to unlock the extreme density and ultra-low power consumption required to power the next generation of autonomous sensing and industrial robotics

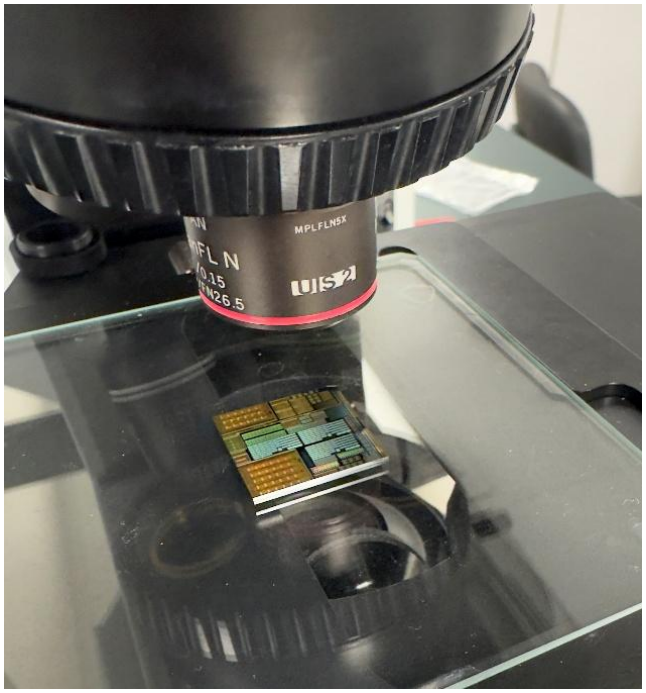

Figure 3: Optical microscope inspection of an RRAM test wafer during materials characterisation.

The Leap to 22nm: Unlocking High-Value Markets

The transition from the 180nm strategic test vehicle to the 22nm production node represents a generational leap in semiconductor capability. While 180nm serves as the critical validation gate for the core hardware architecture, the 22nm node is the primary commercial target, delivering the extreme density, energy efficiency, and thermal robustness required for applications in **exoskeletons** and **industrial robotics**, while also enabling CIM.

This scaling is transformative for the Company's existing revenue-generating business. It enables FDA-cleared EMG and movement sensors to evolve from raw-data streaming devices into autonomous, on-body inference nodes. For exoskeleton and robotics systems, it provides the localized compute power necessary for real-time, low-latency decision-making at the ultra-edge.

The project has explicitly mapped the hardware gains of the 22nm node to its highest-potential commercial sectors:

Target Application Sector	Key Technical Gains at 22nm
Battery-Powered Edge Devices (medical implants, wearables, IoT)	20–30% reduction in write voltage; lower energy cost per operation

High-Speed Sensors and AI Compute (exoskeletons, on-body inference)	More than 2× increase in cell density for larger compute-in-memory arrays; endurance above 10 million program/erase cycles
Industrial Robotics	Data retention above 10 years at 125°C; 40°C improvement in thermal robustness over previous baselines

Neuromorphic and Compute in memory (CIM) Integration

The Company has validated its RRAM architecture as a high-performance computational engine, representing a paradigm shift from traditional data storage to active processing. In alignment with the strategic framework established in the **ASX announcement dated 13 March 2026**, design and layout work has been completed for a compute-in-memory (CIM) macro integrated directly onto the 256Kb array. By executing neural network inference within the memory fabric itself, the platform effectively overcomes the **"Memory Wall"**, the industry-wide bottleneck where 70% to 90% of compute energy is typically wasted moving data between separate processors and external memory.

This hardware layer is designed to integrate seamlessly with the Company's proprietary neuromorphic IP portfolio, including delta-sigma neurons, memristive learning arrays, and adaptive neural converters. This convergence transforms standard movement sensors into intelligent, autonomous nodes capable of local sensing, inference, and real-time decision-making, eliminating the need for constant cloud connectivity or power-hungry external accelerators.

When applied to mission-critical applications such as **wearable robotics**, **exoskeletons**, and **autonomous systems**, this architecture delivers transformative performance gains over traditional raw-data-streaming models:

- **Order-of-Magnitude Energy Efficiency:** Achieving roughly one order of magnitude lower energy consumption per inference, significantly extending operational uptime.
- **Reflex-Grade Responsiveness:** A multi-fold reduction in end-to-end decision latency, providing the sub-millisecond control loops essential for fluid movement and safety in robotics.
- **System Simplification:** A projected **25% to 50% reduction** in the number of sensors required per body, lowering both hardware complexity and total system cost.

- **Doubled Operational Battery Life:** More than double the battery life for the overall system, drastically reducing the frequency of recharging for users in the field.

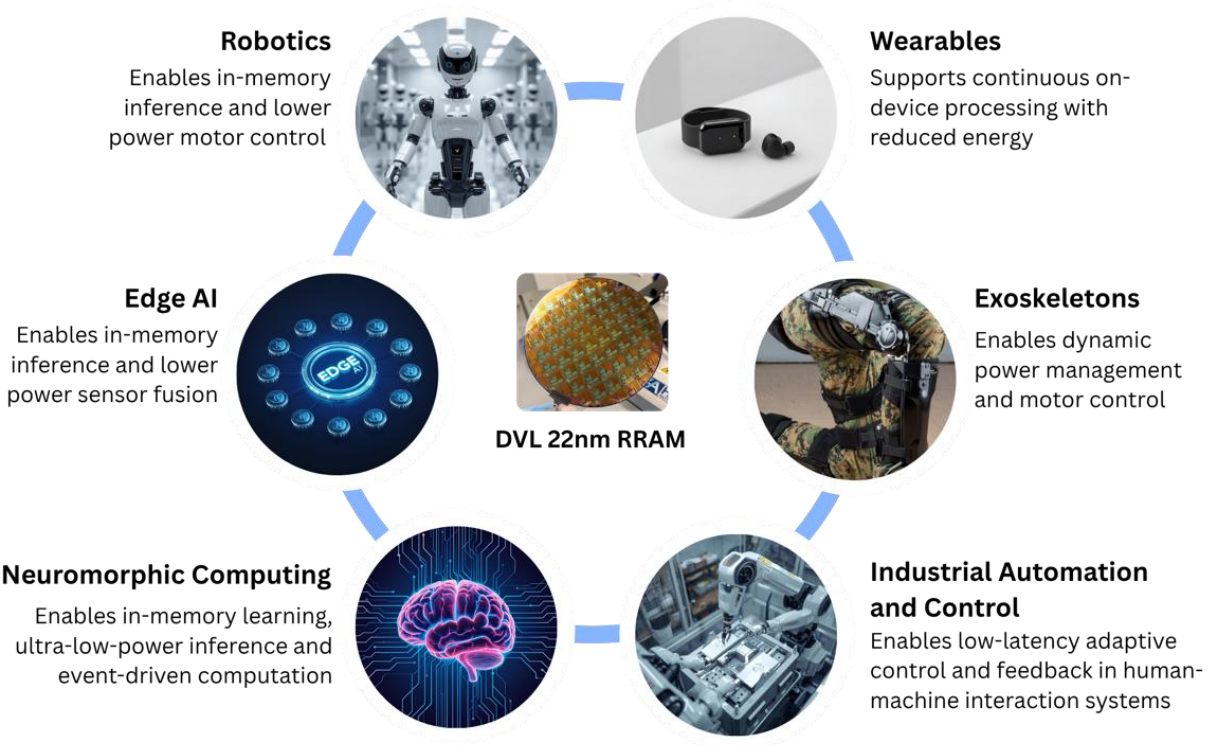

Figure 4: Conceptual image of the companies target applications using the 22nm RRAM technology

Tape-out and next steps

The 180nm RRAM test chip is currently in the final pre-tape-out stage, with submission to a Tier-1 foundry targeted for Q3 2026. This test vehicle serves as a critical validation gate for both the RRAM material stacks and the Compute-in-Memory (CIM) architecture, directly addressing the "Memory Wall" and energy-intensive data movement that currently constrains edge AI.

Both the RRAM and CIM circuit and layout designs are fully completed. Test chip assembly, 256Kb RRAM integration, and final verification processes are nearing conclusion, with Layout Versus Schematic (LVS) confirmed on the MAC array and test keys. A formal design review is scheduled for June 2026, with tape-out targeted shortly thereafter. In parallel, the next lot of development wafers is in production to further optimize integration uniformity.

Following the successful tape-out of the 180nm vehicle, the project will advance into sequential manufacturing and validation phases to support the Company's migration to the high-value 22nm node:

- **Fabrication and Integration:** The project will move into foundry processing, followed by multiple rounds of Back-End-of-Line (BEOL) integration with our world-leading research partners throughout 2027.

- **Device Testing and Optimization:** Extensive characterization will be conducted on the returned silicon to validate performance metrics, long-term reliability, and commercial yield required for autonomous robotics and drones.
- **22nm Design Phase:** Leveraging the validated 180nm architecture, the 22nm test chip design phase is scheduled to commence in **H2 2027**.

Mathew Regan, Group Chief Executive Officer of dorsaVi, said: *"Qualifying three RRAM stacks against commercial foundry standards was the principal technical hurdle in this program, and it is now behind us. BEOL compatibility means we can manufacture on existing CMOS production lines rather than a dedicated facility, which is what supports the unit economics required for production volume. The team is focused on tape-out at a Tier-1 commercial foundry in Q3 2026, with the 22nm design phase commencing in the second half of 2027. For our sensor business, this is the platform that allows our existing FDA-cleared devices to evolve from streaming sensors into local inference nodes."*

The Company is committed to maintaining its technical momentum as it moves toward the definitive commercialization of its hardware platform:

- **Continued Technical Optimization:** The Company will continue testing the qualified material stacks across a range of performance metrics to further characterize and optimize the technology for industrial-grade reliability.
- **Execution of the Tape-Out Milestone:** The program remains on track for the scheduled tape-out in **Q3 2026**, representing a key milestone in the transition to functional semiconductor production.
- **Fusing RRAM with Neuromorphic Intelligence:** A primary focus of the next phase is the strategic integration of RRAM with the Company's proprietary neuromorphic computing capabilities. This convergence targets high-value sectors, including **wearable robotics**, **prosthetics**, and **autonomous sensing systems**.

This release has been authorised for lodgement to the ASX by the Board.

- **ENDS** -

Mathew Regan	**Gernot Abl**
Group Chief Executive Officer	**Chairman**
+61 427 477 298	**+61 419 802 653**
Email: mregan@dorsaVi.com	**Email: ga@dorsaVi.com**

Forward-Looking Statements

This announcement may contain certain forward-looking statements and projections. Such forward-looking statements/projections are estimates for discussion purposes only and should not be relied upon. Forward looking statements/projections are inherently uncertain and may therefore differ materially from results ultimately achieved. dorsaVi Limited does not make any representations and provides no warranties concerning the accuracy of the projections and disclaims any obligation to update or revise any forward-looking statements/projections based on new information, future events or otherwise, except to the extent required by applicable laws.

About dorsaVi

dorsaVi Ltd (ASX: DVL) is an ASX company focused on delivering intelligence at the ultra-edge. Enabling real time AI-driven decisions to be made locally, at the point of sensing, without reliance on cloud connectivity. dorsaVi's wearable sensor technology captures, quantifies, and assesses detailed human movement and position outside a biomechanics lab, in both real-time and real situations for up to 24 hours, across clinical applications, elite sports, and occupational health and safety. Underpinning this vision, dorsaVi is building the hardware foundations of the ultra-edge through strategic investments in neuromorphic computing and RRAM memory technology. dorsaVi's focus is on three major markets:

- Ultra-Edge Intelligence: dorsaVi's sensor platforms are designed to process and act on data locally, embedding AI-driven inference directly at the point of capture. By investing in neuromorphic computing and RRAM memory technology, dorsaVi enables real-time decision-making without round-tripping to the cloud, delivering lower latency, lower power consumption, and reliable operation in latency- and connectivity-constrained environments across industrial, clinical, and autonomous systems applications.
- Workplace: dorsaVi enables employers to assess risk of injury for employees as well as test the effectiveness of proposed changes to OHS workplace design, equipment or methods based on objective evidence. dorsaVi works either directly with major corporations, or through an insurance company's customer base with the aim of reducing workplace compensation and claims. dorsaVi has been used by major corporations including London Underground, Vinci Construction, Crown Resorts, Caterpillar (US), Boeing, Monash Health, Coles, Woolworths, Toll, Toyota, Orora, Mineral Resources and BHP.
- Clinical: dorsaVi is transforming the management of patients with its clinical solutions (ViMove+) which provide objective assessment, monitoring outside the clinic and immediate biofeedback. The clinical market is broken down into physical therapy (physiotherapists), hospital in the home and elite sports. Hospital in the home refers to the remote management of patients by clinicians outside of physical therapy (i.e. for orthopaedic conditions). Elite sports refer to the management and optimisation of athletes through objective evidence for decisions on return to play, measurement of biomechanics and immediate biofeedback to enable peak performance.

Further information is available at www.dorsavi.com