18 June 2026

dorsaVi Finalises Design of RRAM-CMOS Validation Chip, Advancing the Program to Fabrication

Completed design locks in three key capabilities boosting performance and scalability: self-checking write-and-verify, compute-in-memory that computes inside the array, and integration on standard commercial CMOS.

Key Highlights:

- **First RRAM-CMOS validation chip design finalised:** dorsaVi has completed the full design package for its integrated RRAM-CMOS chip, developed in conjunction with NTU Singapore and ITRI Taiwan; the design is ready for fabrication.

- **Self-checking Write-and-Verify Circuit to Improve Memory Reliability:** The chip includes write-and-verify circuitry that checks the programmed RRAM state after each write operation before the data is accepted. This helps reduce marginal writes, improve sensing margin, and strengthen memory reliability for future ultra-edge applications including defence, medical devices, exoskeletons, robotics, and industrial AI.

- **Compute-in-Memory for Future Edge AI:** The chip includes purpose-built Compute-in-Memory macros that allow the same RRAM array to store data and support local accumulation across up to 64 inputs. This validates how future RRAM-based hardware may reduce repeated data movement between memory and processors, a key source of power use and latency in edge devices.

- **Built to scale on semiconductor foundry lines:** the RRAM sits in the chip's back-end-of-line metal layers commercial CMOS front-end wafers sourced through TSMC, followed by partner-led BEOL and RRAM integration. It scales on existing foundry lines, with BEOL-compatible integration using a commercial CMOS foundation.

- **Aimed at high-value markets:** exoskeleton, defence, robotics, industrial AI, and intelligent sensing, each needing local, low-power, non-volatile intelligence on-device.

Melbourne, Australia, 18 June 2026 – dorsaVi Limited (ASX: DVL) ("dorsaVi" or the "Company") is pleased to announce that it has finalised the design package for its first integrated RRAM-CMOS validation chip. With the design complete, the program now moves from final design package into tape-out and staged silicon implementation.

The validation chip is designed to prove three important building blocks for dorsaVi's ultra-edge intelligence roadmap: more reliable RRAM programming through write-and-verify circuitry, local Compute-in-Memory operation using the same RRAM array, and a practical integration pathway that combines commercial CMOS front-end wafers with partner-led BEOL and RRAM process integration. Results are expected to inform the Company's subsequent 22-nm implementation pathway.

Key Feature 1: Write-and-Verify for High Reliability

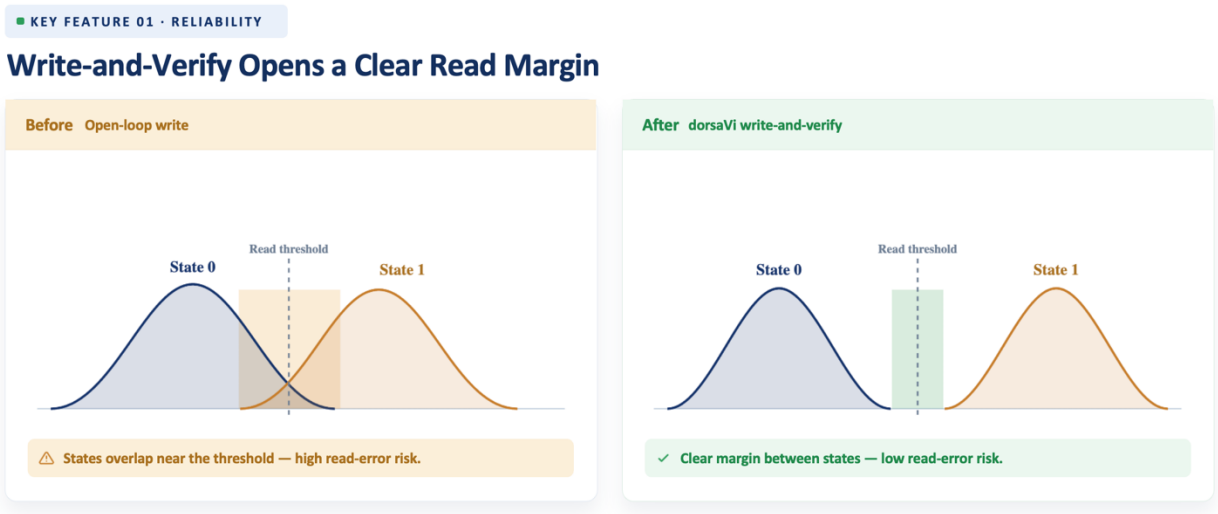

Figure 1: Visual showing how the chip checks each memory cell against an acceptable threshold after writing, and automatically corrects any cell that does not meet it

The Problem – RRAM Programming Variability:

RRAM stores data through resistance states rather than charge storage. In practical array operation, the resistance state reached after a write operation can vary due to device-to-device variation, cycle-to-cycle variation, array parasitics, and operating conditions.

If a programmed cell sits too close to the sensing threshold, the read circuit may have reduced margin when distinguishing between stored "1" and stored "0" states. In larger arrays, these marginal states can increase the need for additional read checks, tighter sensing calibration, or error-management techniques. This is why programming control and resistance-state verification are important steps toward reliable RRAM memory operation.

Our Solution – Write-and-Verify Control:

The implemented write-and-verify circuitry is designed to close the programming loop. After a write operation, the circuit reads back the programmed RRAM state and checks whether it falls within the intended resistance window. If the state is marginal or outside the target window, the circuit can support further tuning or identify the condition for optimisation.

This approach turns RRAM programming from a simple open-loop write event into a more controlled process. It is designed to improve programming accuracy, reduce marginal memory states, increase sensing margin, and provide silicon-level data for future reliability and yield optimisation.

To achieve this, dorsaVi has included dedicated write-and-verify circuitry within the validation chip:

- **Post-Write State Verification:** The circuit reads back the programmed RRAM state after a write operation before the data is treated as successfully programmed.
- **Controlled Re-Programming Path:** If the programmed state does not fall within the intended resistance window, the circuit can support additional tuning or re-programming steps to improve state placement.
- **Improved Sensing Margin:** By reducing the number of marginal cells near the sensing threshold, write-and-verify is expected to support more robust separation between stored "1" and stored "0" states.
- **Reliability and Yield Learning:** The write-and-verify function provides practical silicon data on programming behaviour across the array, supporting future optimisation of write algorithms, sensing schemes, array yield, and long-term memory reliability.

The result is a more reliability-focused RRAM validation architecture for future applications where stable local memory operation is important, including defence, medical devices, exoskeletons, robotics, and industrial AI hardware.

Key Feature 2: Compute-in-Memory for Faster Decisions at Lower Power

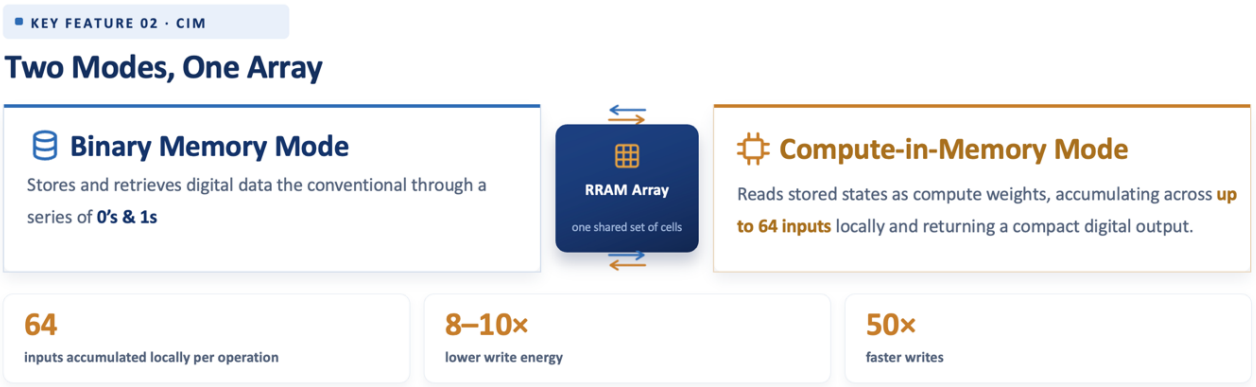

Figure 2: Visual showing how the memory array switches between storing data and running calculations in place, removing the need to move data to a separate processor.

The Problem – Data Movement is Slow and Energy Costly:

In conventional architectures, moving data repeatedly between memory and a separate processor is a major source of power consumption and latency, particularly in edge devices operating under tight energy and response-time constraints.

Our Solution – Give Memory Local Compute Capability:

dorsaVi's Compute-in-Memory design is intended to reduce this repeated data movement by allowing selected compute operations to occur closer to where the data is stored. The same RRAM array that stores programmed resistance states can also be evaluated as a local compute structure, supporting array-level accumulation for future edge-AI and neuromorphic-style workloads.

The design includes purpose-built Compute-in-Memory structures that operate in two modes:

- **Binary Memory Mode:** Stores and retrieves digital data in the conventional way.
- **Compute-in-Memory Mode:** Uses programmed resistance states as compute weights, accumulating across up to 64 inputs locally before producing a compact digital compute output through the CIM readout path.

This architecture is designed to validate how future RRAM-based hardware may reduce the need to repeatedly shuttle data between memory and a separate processor, supporting lower energy consumption and faster local decision-making in future ultra-edge applications.

Key Feature 3: Back-End-of-Line Integration for Scale on Commercial Foundries

Figure 3: Visual showing how the RRAM memory layer is stacked on top of the existing chip circuitry, added after manufacturing without altering the foundry process below.

Rather than requiring changes to the CMOS transistor layer, dorsaVi's RRAM integration is designed around the chip's back-end-of-line (BEOL) metal layers, which sit above the standard CMOS front-end transistor circuitry. This means the validation chip can use commercial CMOS front-end wafers sourced through TSMC, followed by partner-led BEOL and RRAM integration steps.

This integration approach provides four important advantages:

- **Commercial CMOS foundation:** The program uses standard commercial CMOS front-end wafers as the starting point, reducing the need to redesign the underlying transistor platform.
- **BEOL-compatible integration pathway:** The RRAM stack is integrated within the BEOL process flow, supporting evaluation of how the memory layer can be added above the CMOS circuitry while preserving the front-end device structure.
- **Future density scaling potential:** Placing RRAM in the upper integration layers supports a pathway toward higher memory density and more compact memory-compute architectures over time.
- **Scalable manufacturing pathway:** By combining commercial CMOS front-end wafers with partner-led BEOL and RRAM integration, the program is designed to generate practical silicon data needed to support future process optimisation, manufacturability assessment, and node migration.

How These Features Map to High-Value Target Markets

This memory matters wherever a device must decide locally, in real time, on a tight power budget. Representative applications include:

Application Sector	Use Case and Value Proposition
Smart Exoskeletons (Lead Market)	Smart EMG sensor nodes read muscle signals to determine user intent (swing, push-off, fatigue) and send commands instead of streaming raw data. Requires fast writes inside the control loop and non-volatile storage for each user's baseline.
Robotics (Industrial and Humanoid)	Joint controllers run individual position and torque loops and hold calibration. Requires fast mid-loop updates and non-volatile memory that survives power cycles so the limb wakes up calibrated without re-homing.
On-Device Industrial AI	Running a model locally requires weights held non-volatile and next to the compute. Compute-in-Memory and BEOL density allow the model to sit on-die and run without a power-hungry reload.

Next-Steps

With the design package finalised, dorsaVi is advancing the program on three fronts:

- **Tape-out:** The chip proceeds to tape-out as scheduled.
- **Integration into dorsaVi's sensing platform:** Validated silicon will progress toward embedding directly into dorsaVi's wearable sensor hardware, enabling on-device intelligence without external processing.
- **Market evaluation & commercialisation:** dorsaVi will engage with prospective partners and customers across its target markets, including exoskeleton, defence, robotics, and industrial AI, to evaluate fit and progress toward commercial deployment.

CEO Commentary

Mathew Regan, Group Chief Executive Officer of dorsaVi, said:

> *"Finalising the design of our first RRAM-CMOS validation chip is a significant milestone for the program. It confirms the architecture is manufacturable under standard commercial foundry conditions and clears the path to the physical silicon we need to validate performance. We are now focused on fabrication and on using the results to advance the program toward commercial scale."*

This release has been authorised for lodgement to the ASX by the Board.

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Forward-Looking Statements

This announcement may contain certain forward-looking statements and projections. Such forward-looking statements/projections are estimates for discussion purposes only and should not be relied upon. Forward looking statements/projections are inherently uncertain and may therefore differ materially from results ultimately achieved. dorsaVi Limited does not make any representations and provides no warranties concerning the accuracy of the projections and disclaims any obligation to update or revise any forward-looking statements/projections based on new information, future events or otherwise, except to the extent required by applicable laws.

About dorsaVi

dorsaVi Ltd (ASX: DVL) is an ASX company focused on delivering intelligence at the ultra-edge. Enabling real time AI-driven decisions to be made locally, at the point of sensing, without reliance on cloud connectivity. dorsaVi's wearable sensor technology captures, quantifies, and assesses detailed human movement and position outside a biomechanics lab, in both real-time and real situations for up to 24 hours, across clinical applications, elite sports, and occupational health and safety. Underpinning this vision, dorsaVi is building the hardware foundations of the ultra-edge through strategic investments in neuromorphic computing and RRAM memory technology. dorsaVi's focus is on three major markets:

- Ultra-Edge Intelligence: dorsaVi's sensor platforms are designed to process and act on data locally, embedding AI-driven inference directly at the point of capture. By investing in neuromorphic

computing and RRAM memory technology, dorsaVi enables real-time decision-making without round-tripping to the cloud, delivering lower latency, lower power consumption, and reliable operation in latency- and connectivity-constrained environments across industrial, clinical, and autonomous systems applications.

- Workplace: dorsaVi enables employers to assess risk of injury for employees as well as test the effectiveness of proposed changes to OHS workplace design, equipment or methods based on objective evidence. dorsaVi works either directly with major corporations, or through an insurance company's customer base with the aim of reducing workplace compensation and claims. dorsaVi has been used by major corporations including London Underground, Vinci Construction, Crown Resorts, Caterpillar (US), Boeing, Monash Health, Coles, Woolworths, Toll, Toyota, Orora, Mineral Resources and BHP.

- Clinical: dorsaVi is transforming the management of patients with its clinical solutions (ViMove+) which provide objective assessment, monitoring outside the clinic and immediate biofeedback. The clinical market is broken down into physical therapy (physiotherapists), hospital in the home and elite sports. Hospital in the home refers to the remote management of patients by clinicians outside of physical therapy (i.e. for orthopaedic conditions). Elite sports refer to the management and optimisation of athletes through objective evidence for decisions on return to play, measurement of biomechanics and immediate biofeedback to enable peak performance.

Further information is available at www.dorsavi.com