15 July 2026

dorsaVi Commences Tape-Out of Validation Chip, A Key Milestone in 22-nm RRAM Development Pathway

Milestone advances the program from completed design into physical silicon manufacturing to validate dorsaVi's RRAM platform for future AI, robotics, EV and wearable applications

Key Highlights:

- **Tape-out commenced:** DVL has commenced the tape-out process for its first RRAM-CMOS validation chip with tier-one semiconductor partners[1], progressing the program from finalised design package into staged silicon implementation.

- **Significant technical milestone for the 22-nm development:** Represents a significant execution milestone in the Company's 22 nm RRAM development program, progressing from design completion toward fabrication, wafer-level electrical testing and silicon validation

- **Commercial CMOS front-end pathway:** The implementation flow uses commercial CMOS front-end wafers sourced through TSMC, followed by partner-led BEOL and RRAM integration before wafer-level electrical testing.

- **Advanced memory to meet global AI Memory Demand:** DVL's RRAM targets rising edge-AI demand for local, low-power, non-volatile memory, using an architecture designed for standard commercial CMOS processes.

- **Targets high-value markets in need of advanced memory:** Supports dorsaVi's broader roadmap for low-power, local intelligence in future sensing, robotics, exoskeleton, defence, medical/wearable, and industrial AI hardware platforms.

- **Generates Critical Silicon Validation Data:** The validation chip is designed to provide electrical and process data that will guide RRAM integration, circuit optimisation, manufacturing refinement and the Company's planned progression toward future 22 nm RRAM-CMOS development.

Melbourne, Australia – dorsaVi Limited (ASX: DVL) ("dorsaVi" or the "Company") is pleased to announce that, following the recently announced finalisation of its RRAM-CMOS validation chip design, the program has now commenced the tape-out pathway and moved into staged silicon implementation, marking a significant step forward in dorsaVi's RRAM development program.

[1] See ASX Announcement Dated 28th January 2026

This milestone advances the chip from final design package into the physical implementation flow required to produce silicon for wafer-level electrical testing. The validation chip is intended to generate practical silicon data on RRAM-CMOS integration, array operation, write-and-verify behaviour, Compute-in-Memory functionality, and process learning, advancing its deployment across multiple high-value target markets.

From Design Finalisation to Tape-Out Execution

Figure 1: Conceptual flowchart showcasing the process flow from design to tape-out

Tape-out is the process by which the finalised integrated circuit design package is prepared for physical manufacturing. This transition from design to fabrication proves the architecture is ready for standard commercial foundry conditions

The validation chip is intended to provide practical silicon data on RRAM-CMOS integration, memory array operation, write-and-verify behaviour, Compute-in-Memory functionality, sensing behaviour, and wafer-level test methodology. These results are expected to inform future optimisation of the Company's RRAM platform and support its subsequent 22-nm implementation pathway.

Why This is an Important Step

Tape-out represents a critical transition point in the development of an integrated circuit, where a completed design moves into the implementation flow required to produce physical silicon for testing and validation.

This milestone is particularly important because the validation chip is designed to assess how the RRAM memory macro, peripheral circuits, write-and-verify function, Compute-in-Memory structures, sensing paths, and test features behave together under physical silicon conditions.

This milestone serves three purposes:

- **Validation of advanced memory features:** Validating the RRAM memory array, dedicated write-and-verify circuitry, and Compute-in-Memory structures operate together under physical silicon conditions, including resistance-state separation, sensing margin, and CIM readout behaviour.

- **Opens the pathway to high-value applications:** this will allow DVL to progress toward embedding validated silicon into target platforms across exoskeletons, robotics, defence, and industrial AI, each requiring local, low-power, non-volatile intelligence on-device.

- **Scalable manufacturing process:** The implementation uses commercial CMOS front-end wafers and integrates the RRAM stack into existing back-end-of-line (BEOL) flows, supporting the ability to manufacture and scale using established foundry infrastructure.

Pathways to Match Global AI Memory Demand

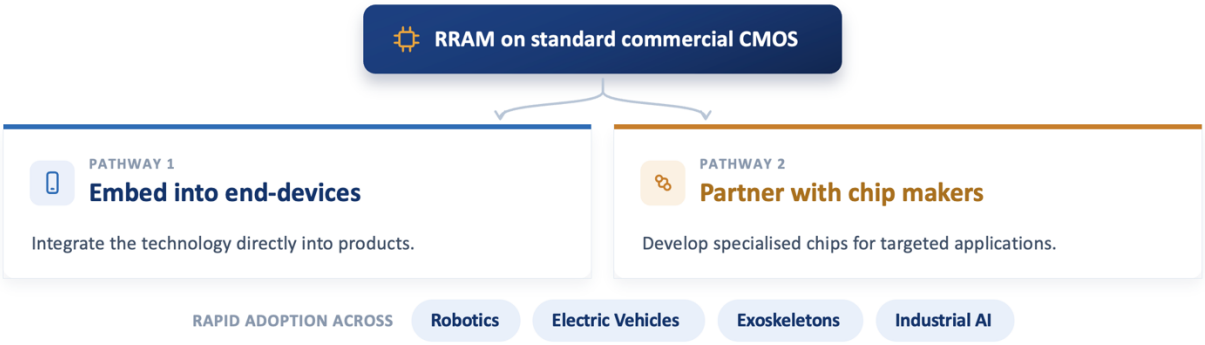

Figure 2: Conceptual diagram showcasing the two potential pathways DVL can address the global AI memory demands through RRAM.

Two Potential Pathways:

That compatibility points to two potential pathways. The first would be embedding the technology directly into end-devices. The second would be working alongside foundries and fabless chip makers to develop specialised chips for targeted applications. Both are intended to be accessible without new manufacturing investment, which could make the technology practical for adoption across robotics, electric vehicles, exoskeletons, and industrial AI.

How the Validation Chip Supports These Pathways:

The validation chip follows a staged silicon implementation pathway. It uses commercial CMOS front-end wafers sourced through TSMC, followed by partner-led BEOL and RRAM integration, before wafer-level

electrical testing. This staged approach allows dorsaVi and its partners to evaluate RRAM integration on a commercial CMOS foundation while preserving flexibility for process learning, electrical test development, and future node migration.

Creating Non-Volatile Memory that Computes

Traditionally, memory and compute have been treated as separate functions, with data shuttled back and forth between the two. By integrating Compute-in-Memory structures directly into the RRAM array, the same physical layer that stores data can also perform calculations locally.

Traditional Memory Bottlenecks:
In conventional architectures, repeatedly moving data between memory and a separate processor is a primary source of power consumption and latency. For edge devices operating under tight energy and response-time constraints, this bottleneck directly limits what the hardware can do.

DVL's Compute-in-Memory Architectures:
By integrating RRAM directly with CMOS on the validation chip, dorsaVi can benchmark and test Compute-in-Memory (CIM) capabilities. This structure allows the memory array to both store data and perform calculations locally.

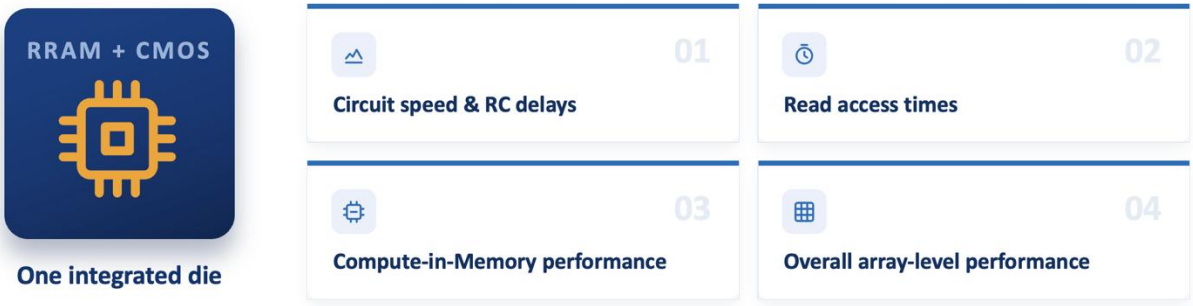

Figure 3:Visual showcasing key performance metrics to be measured on the integrated RRAM-CMOS die

High-Value Markets and Applications Targeted

The validation work supports dorsaVi's broader ultra-edge intelligence roadmap, where local memory, low-power processing, and on-device decision-making are expected to be important for future sensing and hardware platforms.

MARKET	SPECIFIC APPLICATION	HOW RRAM BENEFITS IT
Smart Exoskeletons	EMG-driven intent recognition nodes	Fast writes inside the control loop; non-volatile storage of each user's personalised baseline without cloud dependency.
Robotics	Joint position and torque controllers	Non-volatile memory survives power cycles, so the limb wakes up calibrated without re-homing.
Defence	Autonomous edge sensing platforms	Local inference without connectivity; low power draw extends operational endurance in the field.
Industrial AI	On-device model inference	Model weights held non-volatile and adjacent to compute; eliminates power-hungry data reload cycles.
Medical & Wearables	Continuous biosignal monitoring	Always-on, low-power memory retains patient baselines locally, removing reliance on external processing.

Figure 4: Graphic table showcasing DVL's target applications and the benefits RRAM brings

CEO Commentary

Mathew Regan, Group Chief Executive Officer of dorsaVi, said:

> *"Commencing the tape-out of our first RRAM test-chip is a significant milestone for the program. It confirms that our RRAM architecture is manufacturable under standard commercial foundry conditions and gives us the physical silicon we need to validate performance and refine the technology. We are focused on executing this next phase of testing and using the results to advance the program toward commercial scaling."*

- ENDS -

This release has been authorised for lodgement to the ASX by the Board.

- ENDS –

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Forward-Looking Statements

This announcement may contain certain forward-looking statements and projections. Such forward-looking statements/projections are estimates for discussion purposes only and should not be relied upon. Forward looking statements/projections are inherently uncertain and may therefore differ materially from results ultimately achieved. dorsaVi Limited does not make any representations and provides no warranties concerning the accuracy of the projections and disclaims any obligation to update or revise any forward-looking statements/projections based on new information, future events or otherwise, except to the extent required by applicable laws.

About dorsaVi

dorsaVi Ltd (ASX: DVL) is an ASX company focused on delivering intelligence at the ultra-edge. Enabling real time AI-driven decisions to be made locally, at the point of sensing, without reliance on cloud connectivity. dorsaVi's wearable sensor technology captures, quantifies, and assesses detailed human movement and position outside a biomechanics lab, in both real-time and real situations for up to 24 hours, across clinical applications, elite sports, and occupational health and safety. Underpinning this vision, dorsaVi is building the hardware foundations of the ultra-edge through strategic investments in neuromorphic computing and RRAM memory technology. dorsaVi's focus is on three major markets:

- Ultra-Edge Intelligence: dorsaVi's sensor platforms are designed to process and act on data locally, embedding AI-driven inference directly at the point of capture. By investing in neuromorphic computing and RRAM memory technology, dorsaVi enables real-time decision-making without round-tripping to the cloud, delivering lower latency, lower power consumption, and reliable operation in latency- and connectivity-constrained environments across industrial, clinical, and autonomous systems applications.

- Workplace: dorsaVi enables employers to assess risk of injury for employees as well as test the effectiveness of proposed changes to OHS workplace design, equipment or methods based on objective evidence. dorsaVi works either directly with major corporations, or through an insurance company's customer base with the aim of reducing workplace compensation and claims. dorsaVi has been used by major corporations including London Underground, Vinci Construction, Crown Resorts, Caterpillar (US), Boeing, Monash Health, Coles, Woolworths, Toll, Toyota, Orora, Mineral Resources and BHP.

- Clinical: dorsaVi is transforming the management of patients with its clinical solutions (ViMove+) which provide objective assessment, monitoring outside the clinic and immediate biofeedback. The clinical market is broken down into physical therapy (physiotherapists), hospital in the home and elite sports. Hospital in the home refers to the remote management of patients by clinicians outside of physical therapy (i.e. for orthopaedic conditions). Elite sports refer to the management and optimisation of athletes through objective evidence for decisions on return to play, measurement of biomechanics and immediate biofeedback to enable peak performance.

Further information is available at www.dorsavi.com